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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,732	12/08/2003	Radu Andrei	IMECP018	5107

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EXAMINER	
LAM, DAVID	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,732	ANDREI ET AL.	
	Examiner	Art Unit	
	David Lam	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27 and 28* is/are allowed.

6)☒ Claim(s) *1,2,4-8,10,12-14,19-26,29,30,33 and 35-42* is/are rejected.

7)☒ Claim(s) *3,9,11,15-18,31,32,34,43 and 44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/04, 8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. The improper restriction requirement made in the Office action mailed on 2/24/05 is hereby withdrawn.

Claim Objections

2. Claims 12, 20-21, are objected to because of the following informalities:

- In claim 12, line 2, "at least one other one of the levels" should be change to -- at least one of the level --;
- In claim 20, line 2, "inter-level" should be change to -- intra-level --;
- In claim 21, line 1, "any of a semiconductor" should be change to -- any one of a semiconductor --. Appropriate correction is required.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 29-35-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Nejad et al. (US 2003/0214835).

Regarding to claims 29, 35-42, Nejad et al. disclose a three dimensional circuit comprising a plurality of stacked levels on a substrate, each level comprising a plurality of circuit modules (908) having substantially identical dimension arranged in a contiguous, two dimensional array, each circuit module comprises a plurality of metal circuit component, a level of interconnection (32) for providing interconnections between the circuit modules on different ones of the plurality of stacked levels; wherein the plurality of circuit modules comprises substantially identical and interchangeable memory array modules, each array module comprises all-metal cells, support electronics (12, 16) are deployed in separate layers/single layer of the memory array mode and operable to facilitate access to the array of memory cells; wherein the

substrate is a semiconductor substrate and comprises support electronics (12, 16) for facilitating access to the memory array modules. *See Figs. 1-4; Pages 2-4.*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 4-8, 10, 12-14, 19-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nejad et al. (US 2003/0214835).

Regarding to claims 1-2, 4-6, Nejad et al. disclose a three dimensional circuit comprising: a plurality of stacked levels (34) on a substrate, each level comprising a plurality of metal circuit components and arranged in two dimensions, an interconnect (32) for providing interconnection between the circuit components on different ones of the plurality of levels, wherein at least on of the levels comprise a plurality of memory cells, each memory cell comprising a multi-layer structure magnetoresistance; a semiconductor level among the plurality of the stacked levels, wherein the substrate comprises the semiconductor level and the semiconductor level comprises support electronics (12, 16) for controlling access to the plurality of memory cells. *See Figs. 1-4; Pages 2-4.*

Regarding to claims 7-8, 10, Nejad et al. disclose wherein the plurality of memory cells are arranged in a plurality of substantially identical and interchangeable memory array modules,

each array module comprises metal support electronics (12, 16) for controlling access to the corresponding memory array module/plurality of memory cells. *See Figs. 1-4; Pages 2-4.*

Regarding to claims 12-14, Nejad et al. disclose wherein the plurality of circuit components on at least one of the level comprise metal support electronics are arranged on separate/combined on selected ones of stacked levels (12, 16) for controlling access to the plurality of memory cells. *See Figs. 1-4; Pages 2-4.*

Regarding to claims 19-22, Nejad et al. discloses wherein the interconnect (32, 33) comprises a plurality of intra-level interconnect structures (33), each corresponding to one of the stacked levels and providing first connection among the circuit components on the corresponding level; at least one inter-level interconnect structure (32) for providing second connections among the intra-level interconnect structures, wherein the at lest one inter-level interconnect structure provides a portion of the second connections between selected ones of the intra-level interconnect structures; wherein an electronic system comprising the three-dimensional circuit and the substrate-comprise any ones of a semiconductor, a metal, and a dielectric. *See Figs. 1-4; Pages 2-4.*

As per above discussion (claims 1-2, 4-8, 10, 12-14, 19-22), Nejad et al. disclose the claimed in invention as noted above but not explicitly disclose wherein the components/cells exhibiting giant magnetoresistance. However, it would have been obvious to one having ordinary skill in the art to form exhibiting giant magnetoresistance of Nejad et al.'s MRAM to

provide a high-speed driving capability, high reliable and easy to write memory device capable of large variations in the magnetoresistive value using small magnetic fields. *Note. Figs. 5-6 of Koganei et al. cited to support well-known position.*

Regarding to of claims 23, 24, Nejad et al. disclose a system/three-dimensional circuit comprising a plurality of stack levels (34) on a substrate, each level comprising a plurality of metal memory cells arranged in two dimensions, each memory cell comprising a multi-layer structure magnetoresistance, the structure further comprising support electronics (32) for controlling access of the memory cells, logic and processing circuitry (CPU), an interconnect (32) for providing interconnection between the circuit components on different ones of the plurality levels. *See Figs. 1-4; Pages 2-4.*

As of claims 25-26, Nejad et al. disclose a system/three-dimensional circuit comprising a plurality of stack levels (34) on a substrate, each level comprising a plurality of metal circuit components arranged in two dimensions, the circuit components forming logic and processing circuitry (CPU), the circuit further comprising an interconnect (32) for providing interconnections between the circuit component on different ones of the plurality levels. *See Figs. 1-4; Pages 2-4.*

Although Nejad et al. does not explicitly discloses wherein the circuit components comprising analog circuitry. However, Nejad et al. disclose the processing system (900) suitable for use on a personal computer, workstation that would inherently including an analog circuitry.

As per above discussion (claims 23-26), Nejad et al. disclose the claimed in invention as noted above but not explicitly disclose wherein each of the memory cell comprising a multi-layer structure exhibiting magnetoresistance and the circuit components exhibiting giant magnetoresistance. However, it would have been obvious to one having ordinary skill in the art to form exhibiting giant magnetoresistance of Nejad et al.'s MRAM to provide a high-speed driving capability, high reliable and easy to write memory device capable of large variations in the magnetoresistive value using small magnetic fields. *Note. Figs. 5-6 of Koganei et al. cited to support well-known position.*

Regarding to claims 30, 33, Nejad et al. further disclose wherein the circuit components comprise memory cells, each comprising a multi-layer structure; and wherein the circuit components comprise active circuit components, each being operable to generate an output signal.

As per above discussion (claims 30, 33), Nejad et al. disclose the claimed in invention as noted above but not explicitly disclose wherein each of the memory cell comprising a multi-layer structure exhibiting magnetoresistance and each active circuit component being operable base on exhibiting giant magnetoresistance effect. However, it would have been obvious to one having ordinary skill in the art to form exhibiting giant magnetoresistance of Nejad et al.'s MRAM to provide a high-speed driving capability, high reliable and easy to write memory device capable of large variations in the magnetoresistive value using small magnetic fields. *Note. Figs. 5-6 of Koganei et al. cited to support well-known position.*

Allowable Subject Matter

6. Claims 3, 9, 11, 15-18, 31-32, 34, 43-44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is an examiner's statement of reasons for allowance: Claims 27-28 are allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach: a memory system comprising: support electronics, among others as claimed in independent claim 27, comprising a plurality of active circuit components that operable to generate an output signal which is a function of a resistive imbalance among the thin-film elements and which is proportional to a power current in a network of the thin-film elements.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Nishimura (6,104,632) disclose a magnetic thin film memory and recording and reproducing method and apparatus using such a memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Lam whose telephone number is 571-272-1782. The examiner can normally be reached on 6:00 – 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DAVID LAM
PRIMARY EXAMINER

D. Lam

May 16, 2005